**PLUS16R8D/-7 SERIES**

### FEATURES
- Ultra high-speed
  - $t_{PD} = 7.5\text{ns}$ and $f_{\text{MAX}} = 74\text{MHz}$ for the PLUS16R8-7 Series
  - $t_{PD} = 10\text{ns}$ and $f_{\text{MAX}} = 60\text{MHz}$ for the PLUS16R8D Series
- 100% functionally and pin-for-pin compatible with industry standard 20-pin PAL ICs
- Power-up reset function to enhance state machine design and testability
- Design support provided via SNAP and other CAD tools for Series 20 PAL devices
- Field-programmable on industry standard programmers
- Security fuse
- Individual 3-State control of all outputs

### DESCRIPTION
The Philips Semiconductors PLUS16XX family consists of ultra high-speed 7.5ns and 10ns versions of Series 20 PAL devices.

The PLUS16XX family is 100% functional and pin-compatible with the 16L8, 16R8, 16R6, and 16R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 programmable AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLUS16R8, R6, and R4 have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to Active-Low after a specific period of time.

The Philips Semiconductors State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

The PLUS16XX family of devices is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer chart for qualified programmers.

The SNAP software package from Philips Semiconductors supports easy design entry for the PLUS16XX series as well as other PLD devices from Philips Semiconductors. The PLUS16XX series are also supported by other standard CAD tools for PAL-type devices.

Order codes are listed in the Ordering Information table.

### DEVICE NUMBER

<table>
<thead>
<tr>
<th>DEVICE NUMBER</th>
<th>DEDICATED INPUTS</th>
<th>COMBINATORIAL OUTPUTS</th>
<th>REGISTERED OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLUS16L8</td>
<td>10</td>
<td>8 (6 I/O)</td>
<td>0</td>
</tr>
<tr>
<td>PLUS16R8</td>
<td>8</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>PLUS16R6</td>
<td>8</td>
<td>2 I/O</td>
<td>6</td>
</tr>
<tr>
<td>PLUS16R4</td>
<td>8</td>
<td>4 I/O</td>
<td>4</td>
</tr>
</tbody>
</table>

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>ORDER CODE</th>
<th>DRAWING NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>20-Pin Plastic Dual-In-Line 300mil-wide</td>
<td>PLUS16R8DN</td>
<td>0408B</td>
</tr>
<tr>
<td></td>
<td>PLUS16R6DN</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLUS16R4DN</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLUS16L8DN</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLUS16L8–7N</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLUS16R8–7N</td>
<td></td>
</tr>
<tr>
<td>20-Pin Plastic Leaded Chip Carrier (PLCC)</td>
<td>PLUS16R8DA</td>
<td>0400E</td>
</tr>
<tr>
<td></td>
<td>PLUS16R6DA</td>
<td></td>
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<tr>
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<td>PLUS16R4DA</td>
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</tr>
<tr>
<td></td>
<td>PLUS16L8DA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLUS16R8–7A</td>
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</tr>
<tr>
<td></td>
<td>PLUS16R6–7A</td>
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</tr>
<tr>
<td></td>
<td>PLUS16R4–7A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLUS16L8–7A</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:**
The PLUS16XX series of devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Philips Semiconductors Military Data Book.

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September 10, 1993
**PIN CONFIGURATIONS**

**PLUS16L8**

- I0: Dedicated Input
- I1: Dedicated Input
- I2: Dedicated Input
- I3: Dedicated Input
- I4: Dedicated Input
- I5: Dedicated Input
- I6: Dedicated Input
- I7: Dedicated Input
- I8: Dedicated Input
- GND: Ground
- Q7: Registered output
- Q6: Registered output
- B5: Bidirectional (input/output)
- B4: Bidirectional (input/output)
- B3: Bidirectional (input/output)
- B2: Bidirectional (input/output)
- B1: Bidirectional (input/output)
- B0: Registered output
- OE: Output Enable
- VCC: Supply Voltage

**PLUS16R8**

- I0: Dedicated Input
- I1: Dedicated Input
- I2: Dedicated Input
- I3: Dedicated Input
- I4: Dedicated Input
- I5: Dedicated Input
- I6: Dedicated Input
- I7: Dedicated Input
- I8: Dedicated Input
- GND: Ground
- Q7: Registered output
- Q6: Registered output
- B5: Bidirectional (input/output)
- B4: Bidirectional (input/output)
- B3: Bidirectional (input/output)
- B2: Bidirectional (input/output)
- B1: Bidirectional (input/output)
- B0: Registered output
- OE: Output Enable
- VCC: Supply Voltage

**SYMBOL**

- I: Dedicated Input
- O: Dedicated combinatorial Output
- Q: Registered output
- B: Bidirectional (input/output)
- CLK: Clock input
- OE: Output Enable
- VCC: Supply Voltage
- GND: Ground
PIN CONFIGURATIONS

**PLUS16R6**

- **CLK** Clock input
- **I** Dedicated Input
- **I0** Dedicated Input
- **I1** Dedicated Input
- **I2** AND OR ARRAY
- **I3** AND OR ARRAY
- **I4** AND OR ARRAY
- **I5** AND OR ARRAY
- **I6** AND OR ARRAY
- **I7** GND
- **O** Dedicated combinatorial Output
- **Q1** Registered output
- **Q2** Registered output
- **Q3** Registered output
- **Q4** Registered output
- **Q5** Registered output
- **Q6** Registered output
- **Q7** Registered output
- **Q8** Registered output
- **Q9** Registered output
- **Q10** Registered output
- **Q11** Registered output
- **Q12** Registered output
- **Q13** Registered output
- **Q14** Registered output
- **Q15** Registered output
- **Q16** Registered output
- **Q17** Registered output
- **Q18** Registered output
- **Q19** Registered output
- **Q20** Registered output
- **VCC** Supply Voltage
- **GND** Ground

**PLUS16R4**

- **CLK** Clock input
- **I** Dedicated Input
- **I0** Dedicated Input
- **I1** Dedicated Input
- **I2** AND OR ARRAY
- **I3** AND OR ARRAY
- **I4** AND OR ARRAY
- **I5** AND OR ARRAY
- **I6** AND OR ARRAY
- **I7** AND OR ARRAY
- **O** Dedicated combinatorial Output
- **Q1** Registered output
- **Q2** Registered output
- **Q3** Registered output
- **Q4** Registered output
- **Q5** Registered output
- **Q6** Registered output
- **Q7** Registered output
- **Q8** Registered output
- **Q9** Registered output
- **Q10** Registered output
- **Q11** Registered output
- **Q12** Registered output
- **Q13** Registered output
- **Q14** Registered output
- **Q15** Registered output
- **Q16** Registered output
- **Q17** Registered output
- **Q18** Registered output
- **Q19** Registered output
- **Q20** Registered output
- **VCC** Supply Voltage
- **GND** Ground
NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. Programmable connections.
NOTES:
1. All unprogrammed or virgin “AND” gate locations are pulled to logic “0”.
2. Programmable connections.
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2. Programmable connections.
NOTES:
1. All unprogrammed or virgin “AND” gate locations are pulled to logic “0”.
2. Programmable connections.
**FUNCTIONAL DESCRIPTIONS**

The PLUS16XX series utilizes the familiar sum-of-products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLUS16XX series consists of four PAL-type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLUS16L8 is a combinatorial part with 8 user configurable outputs (6 bidirectional), while the other three devices, PLUS16R8, PLUS16R6, PLUS16R4, have respectively 8, 6, and 4 output registers.

**3-State Outputs**

The PLUS16XX series devices also feature 3-State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (On) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

**Programmable Bidirectional Pins**

The PLUS16XX products feature variable Input/Output ratios. In addition to 8 dedicated inputs, each combinatorial output pin of the registered devices can be individually programmed as an input or output. The PLUS16L8 provides 10 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

**Output Registers**

The PLUS16R8 has 8 output registers, the 16R6 has 6, and the 16R4 has 4. Each output register is a D-type flip-flop which is loaded on the Low-to-High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

**Power-up Reset**

By resetting all flip-flops to a logic Low, as the power is turned on, the PLUS16R8, R6, R4 enhance state machine design and initialization capability.

**Software Support**

Like other Programmable Logic Devices from Philips Semiconductors, the PLUS16XX series are supported by SLICE, the PC-based software development tool from Philips Semiconductors. The PLUS16XX family of devices are also supported by standard CAD tools for PAL devices, including ABEL and CUPL. SLICE is available free of charge to qualified users.

**Logic Programming**

The PLUS16XX series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLUS16XX architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

**Programming/Software Support**

Ref to Section 9 (Development Software) and Section 10. (Third-Party Programmer/Software Support) of the PLD data handbook for additional information.

---

<table>
<thead>
<tr>
<th>AND ARRAY – (I, B)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Diagram" /></td>
</tr>
</tbody>
</table>

**VIRGIN STATE**

A factory shipped virgin device contains all fusible links intact, such that:
1. All outputs are at "H" polarity.
2. All $P_n$ terms are disabled.
3. All $P_n$ terms are active on all outputs.

---

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.
### Absolute Maximum Ratings¹

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>–0.5</td>
<td>+7</td>
<td>V DC</td>
</tr>
<tr>
<td>VIN</td>
<td>Input voltage</td>
<td>–1.2</td>
<td>+8.0</td>
<td>V DC</td>
</tr>
<tr>
<td>VOUT</td>
<td>Output voltage</td>
<td>–0.5</td>
<td>VCC + 0.5V</td>
<td>V DC</td>
</tr>
<tr>
<td>IIN</td>
<td>Input currents</td>
<td>–30</td>
<td>+30</td>
<td>mA</td>
</tr>
<tr>
<td>IOUT</td>
<td>Output currents</td>
<td></td>
<td>+100</td>
<td>mA</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage temperature range</td>
<td>–65</td>
<td>+150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTE:**

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

### Thermal Ratings

<table>
<thead>
<tr>
<th>TEMPERATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum junction</td>
</tr>
<tr>
<td>Maximum ambient</td>
</tr>
<tr>
<td>Allowable thermal rise ambient to junction</td>
</tr>
</tbody>
</table>

### Operating Ranges

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>+4.75</td>
<td>+5.25</td>
<td>V DC</td>
</tr>
<tr>
<td>TAMBI</td>
<td>Operating free-air temperature</td>
<td>0</td>
<td>+75</td>
<td>°C</td>
</tr>
</tbody>
</table>
## DC ELECTRICAL CHARACTERISTICS

$0^\circ C \leq T_{\text{amb}} \leq +75^\circ C$, $4.75 \leq V_{\text{CC}} \leq 5.25V$

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$V_{\text{CC}}$</td>
<td>MIN</td>
</tr>
<tr>
<td>$V_{\text{IL}}$</td>
<td>Low</td>
<td>$V_{\text{CC}} = \text{MIN}$</td>
<td>0.8</td>
</tr>
<tr>
<td>$V_{\text{IH}}$</td>
<td>High</td>
<td>$V_{\text{CC}} = \text{MAX}$</td>
<td>2.0</td>
</tr>
<tr>
<td>$V_{\text{IC}}$</td>
<td>Clamp</td>
<td>$V_{\text{CC}} = \text{MIN}, I_{\text{IN}} = -18\text{mA}$</td>
<td>-0.8</td>
</tr>
</tbody>
</table>

### Output voltage

| $V_{\text{OL}}$ | Low | $V_{\text{CC}} = \text{MIN}, V_{\text{IN}} = V_{\text{IH}}$ or $V_{\text{IL}}$ | 0.5 | V |  |
| $V_{\text{OH}}$ | High | I$\text{O}_{\text{L}} = 24\text{mA}$ | 2.4 | V |  |

### Input current

| $I_{\text{IL}}$ | Low$^3$ | $V_{\text{CC}} = \text{MAX}$ | -250 | $\mu A$ |  |
| $I_{\text{IH}}$ | High$^3$ | $V_{\text{IN}} = 2.7V$ | 25 | $\mu A$ |  |
| $I_{\text{I}}$ | Maximum input current | $V_{\text{IN}} = V_{\text{CC}} = V_{\text{CCMAX}}$ | 100 | $\mu A$ |  |

### Output current

| $I_{\text{OZH}}$ | Output leakage | $V_{\text{CC}} = \text{MAX}$ | 100 | $\mu A$ |  |
| $I_{\text{OZL}}$ | Output leakage | $V_{\text{OUT}} = 0V$ | -100 | $\mu A$ |  |
| $I_{\text{OS}}$ | Short circuit$^4,5$ | $V_{\text{OUT}} = 0V$ | -90 | mA |  |
| $I_{\text{IC}}$ | $V_{\text{CC}}$ supply current | $V_{\text{CC}} = \text{MAX}$ | 160 | mA |  |

### Capacitance$^6$

| $C_{\text{IN}}$ | Input | $V_{\text{CC}} = 5V$ | 8 | pF |  |
| $C_{\text{B}}$ | I/O (B) | $V_{\text{OUT}} = 2V, f = 1\text{MHz}$ | 8 | pF |  |

### NOTES:

1. All typical values are at $V_{\text{CC}} = 5V$, $T_{\text{amb}} = +25^\circ C$.
2. All voltage values are with respect to network ground terminal.
3. Leakage current for bidirectional pins is the worst case of $I_{\text{IL}}$ and $I_{\text{OZL}}$ or $I_{\text{IH}}$ and $I_{\text{OZH}}$.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. These parameters are not 100% tested but periodically sampled.
# AC ELECTRICAL CHARACTERISTICS

**R₁ = 200Ω, R₂ = 390Ω, 0°C ≤ Tₘᵦ ≤ +75°C, 4.75 ≤ V₉C ≤ 5.25V**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>FROM</th>
<th>TO</th>
<th>LIMITS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>FROM</td>
<td>TO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MIN¹</td>
<td>TYP</td>
</tr>
<tr>
<td>Pulse Width</td>
<td>Clock High</td>
<td>CK+</td>
<td>CK−</td>
<td>5</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>Clock Low</td>
<td>CK−</td>
<td>CK+</td>
<td>5</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>Period</td>
<td>CK+</td>
<td>CK+</td>
<td>10</td>
<td>14</td>
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</tbody>
</table>

**Setup & Hold time**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>FROM</th>
<th>TO</th>
<th>LIMITS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Input</td>
<td>CK+</td>
<td></td>
<td>0</td>
<td>0</td>
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<td></td>
<td>Input</td>
<td>CK+</td>
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<td></td>
<td>Input</td>
<td>CK+</td>
<td></td>
<td>7</td>
<td>9</td>
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</table>

**Propagation delay**

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>FROM</th>
<th>TO</th>
<th>LIMITS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Clock</td>
<td>CK±</td>
<td>Q±</td>
<td>3</td>
<td>6.5</td>
</tr>
<tr>
<td></td>
<td>Clock³</td>
<td>CK±</td>
<td>Q±</td>
<td>3</td>
<td>6.5</td>
</tr>
<tr>
<td></td>
<td>Output (16L8, R6, R4)²</td>
<td>I, B</td>
<td>Output</td>
<td>3</td>
<td>7.5</td>
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<tr>
<td></td>
<td>Output enable⁴</td>
<td>OE</td>
<td>Output enable</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Output disable⁴</td>
<td>OE</td>
<td>Output disable</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Output enable⁴,⁵</td>
<td>I</td>
<td>Output enable</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Output disable⁴,⁵</td>
<td>I</td>
<td>Output disable</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Output enable ⁴</td>
<td>OE</td>
<td>Output enable</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Output disable ⁴</td>
<td>OE</td>
<td>Output disable</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Output enable</td>
<td>OE</td>
<td>Output enable</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Output disable</td>
<td>OE</td>
<td>Output disable</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Power-Up Reset</td>
<td>VCC+</td>
<td>Q+</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

**Frequency (16R8, R6, R4)**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>FROM</th>
<th>TO</th>
<th>LIMITS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No feedback 1/ (tCKL + tCKH)⁶</td>
<td></td>
<td></td>
<td>100</td>
<td>71.4</td>
</tr>
<tr>
<td></td>
<td>Internal feedback 1/ (tIS + tCKF)⁶</td>
<td></td>
<td></td>
<td>90</td>
<td>64.5</td>
</tr>
<tr>
<td></td>
<td>External feedback 1/ (tIS + tCKO)⁶</td>
<td></td>
<td></td>
<td>74</td>
<td>60.6</td>
</tr>
</tbody>
</table>

---

### NOTES:

1. CL = 0pF while measuring minimum output delays.
2. tPD test conditions: CL = 50pF (with jig and scope capacitance), VIH = 3V, VIL = 0V, VOH = VOL = 1.5V.
3. tCKF was calculated from measured fMAX.
4. For 3-State output; output enable times are tested with CL = 50pF to the 1.5V level, and S₁ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with CL = 5pF. High-to-High impedance tests are made to an output voltage of V₉ (VCCH = 0.5V) with S₁ open, and Low-to-High impedance tests are made to the V₉ (VOL + 0.5V) level with S₁ closed.
5. Same function as tOE₁ and tOD₁, with the difference of using product term control.
6. Not 100% tested, but calculated at initial characterization and at any time a modification in design takes place which may affect the frequency.

---

*For definitions of the terms, please refer to the Timing/Frequency Definitions tables.*

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Philips Semiconductors Programmable Logic Devices

**PAL devices**

16L8, 16R8, 16R6, 16R4

PLUS16R8D/-7 SERIES

September 10, 1993

Page 46
TEST LOAD CIRCUIT

NOTE:
C1 and C2 are to bypass VCC to GND.

OUTPUT REGISTER SKEW

CLOCK TO FEEDBACK PATH
NOTES:
1. Input pulse amplitude is 0V to 3V.
2. Input rise and fall times are 2.5ns.
OUTPUT REGISTER PRELOAD

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With $V_{CC}$ at 5V and Pin 1 at $V_{IL}$, raise Pin 11 to $V_{IHH}$.
Step 2. Apply either $V_{IL}$ or $V_{IH}$ to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to $V_{IL}$. Preload can be verified by observing the voltage level at the output pin.

NOTE: $t_d = t_{SU} = t_{W} = 100\text{ns}$ to $1000\text{ns}$.

$V_{IHH} = 10.25V$ to $10.75V$.

Pin number references for DIP package.
PROGRAMMING/SOFTWARE
Refer to Section 9 (Development Software) and Section 10 (Third-Party Programmer/Software Support) of this data handbook for additional information.

SNAP RESOURCE SUMMARY DESIGNATIONS

PLUS16L8

PLUS16R8
SNAP RESOURCE SUMMARY DESIGNATIONS (Continued)

**PLUS16R8D/-7-series PAL devices**

- **16L8, 16R8, 16R6, 16R4**

**Programmable and Array**

- **I0 – I7**
- **DINPAL7, NINPAL7**
- **B0, B7**
- **Q1 – Q6**
- **Q2 – Q5**

**PLUS16R6**

- **I0 – I7**
- **DINPAL7, NINPAL7**
- **B0, B1, B6, B7**
- **Q1 – Q6**

**PLUS16R4**

- **I0 – I7**
- **DINPAL7, NINPAL7**
- **B0, B1, B6, B7**
- **Q2 – Q5**

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