ADC9708
6-Channel 8-Bit \( \mu \)P Compatible A/D Converter

General Description
The ADC9708 is a single slope 8-bit, 6-channel ADC sub-system that provides all of the necessary analog functions for a microprocessor-based data control system. The device uses an external microprocessor system to provide the necessary addressing, timing and counting functions and includes a 1-of-8 decoder, 8-channel analog multiplexer, sample and hold, ramp integrator, precision ramp reference, and a comparator on a single monolithic chip.

Features
- MPU compatible
- Excellent linearity over full temperature range ±0.2% maximum
- Typical 300 \( \mu \)s conversion time per channel
- Wide dynamic range includes ground
- Auto-zero and full-scale correction capability
- Ratiometric conversion—no precision reference required
- Single-supply operation
- TTL compatible
- Does not require access to data bus or address bus

Connection Diagram

Ordering Information

<table>
<thead>
<tr>
<th>Commercial (0°C ≤ ( T_A ) ≤ 70°C)</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC9708CCN</td>
<td>N16E</td>
</tr>
<tr>
<td>ADC9708CCJ</td>
<td>J16A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Military (−55°C ≤ ( T_A ) ≤ 125°C)</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC9708CMJ</td>
<td>J16A</td>
</tr>
</tbody>
</table>

Block Diagram
Absolute Maximum Ratings (Notes 1, 2)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{CC}$) 18V
Comparator Output (Ramp Stop) $-0.3V$ to $+18V$
Analog Input Range $-0.3V$ to $+30V$
Digital Input Range $-0.3V$ to $+30V$
Output Sink Current 10 mA
Storage Temperature Range $-65°C$ to $+150°C$
Continuous Total Dissipation (Note 8)
  - Ceramic DIP Package 900 mW
  - Molded DIP Package 1000 mW
ESD Susceptibility (Note 9) TBD

Operating Ratings (Notes 1, 2)

Operating Temperature Range
  - ADC9708CCN, ADC9708CCJ $0°C$ to $+70°C$
  - ADC9708CMJ $-55°C$ to $+125°C$
Supply Voltage ($V_{CC}$) 4.75V to 15V
Reference Voltage ($V_{REF}$) (Note 3) $2.8V$ to $5.25V$
Ramp Capacitor ($C_H$) 300 pF
Reference Current ($I_{REF}$) 12 µA to 50 µA
Analog Input Range 0V to $V_{REF}$
Ramp Stop Output Current 1.6 mA

Electrical Characteristics
Over recommended operating conditions, $V_{CC} = 5.0V$, $-55°C \leq T_A \leq +125°C$ for ADC9708CMJ and $0°C \leq T_A \leq +70°C$ for ADC9708CCJ or ADC9708CCN, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical (Note 10)</th>
<th>Limit (Note 11)</th>
<th>Units (Limit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_A$</td>
<td>Conversion Accuracy</td>
<td>Over Entire Temperature Range (Note 4)</td>
<td>$\pm 0.2$</td>
<td>$\pm 0.3$</td>
<td>% (max)</td>
</tr>
<tr>
<td>$E_R$</td>
<td>Linearity</td>
<td>Applies to Any One Channel (Note 5)</td>
<td>$\pm 0.08$</td>
<td>$\pm 0.2$</td>
<td>% (max)</td>
</tr>
<tr>
<td>$V_{OSM}$</td>
<td>Multiplexer Input Offset Voltage</td>
<td>Channel ON, $T_A = -25°C$</td>
<td>2.0</td>
<td>4.0</td>
<td>mV (max)</td>
</tr>
<tr>
<td>$I_C$</td>
<td>Conversion Time per Channel</td>
<td>Channel ON</td>
<td>2.0</td>
<td>7.0</td>
<td>mV (max)</td>
</tr>
<tr>
<td>$I_A$</td>
<td>Acquisition Time</td>
<td>$C_H = 1000$ pF, $I_{REF} = 50$ µA</td>
<td>296</td>
<td>350</td>
<td>µs (max)</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Comparator Logic “1” Output Leakage Current</td>
<td>$V_{OH} = 15V$</td>
<td>1.0</td>
<td>3.0</td>
<td>µA (max)</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Comparator Logic “0” Output Voltage</td>
<td>$I_{OL} = 1.6$ mA</td>
<td>10</td>
<td></td>
<td>µA (max)</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>(Note 6)</td>
<td>40</td>
<td></td>
<td>dB (min)</td>
</tr>
<tr>
<td>Cross Talk between Any Two Channels</td>
<td>(Note 7)</td>
<td>60</td>
<td></td>
<td>dB (min)</td>
<td></td>
</tr>
</tbody>
</table>

Pin Temperature
  - Ceramic DIP (Soldering, 60 Sec.) 300°C
  - Molded DIP (Soldering, 10 Sec.) 260°C
Electrical Characteristics

Over recommended operating conditions, $V_{CC} = 5.0V, -55^\circ C < T_A < +125^\circ C$ for ADC9708CMJ and $0^\circ C < T_A < +70^\circ C$ for ADC9708CCJ or ADC9708CCN; unless otherwise specified. (Continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical (Note 10)</th>
<th>Limit (Note 11)</th>
<th>Units (Limit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>Power Supply Current</td>
<td>$V_{CC} = 5V$ to $15V$, I0 $= 0$</td>
<td>7.5</td>
<td>15</td>
<td>mA (max)</td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td></td>
<td>3.0</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Comparator Output Capacitance</td>
<td></td>
<td>5.0</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: $V_{REF}$ should not exceed $V_{CC} - 2V$.

Note 4: Conversion accuracy is defined as the deviations from a straight line drawn between the points defined by channel address 000 (0 scale) and channel address 111 (full scale) for all channels.

Note 5: Linearity is defined as the deviation from a straight line drawn between the 0 and full scale points for each channel.

Note 6: Power supply rejection ratio is defined as the conversion error contributed by power supply voltage variations while resolving mid scale on any channel.

Note 7: Cross Talk between channels = $20 \log_{10} \frac{D_{VCH}}{D_{VI}}$.

Note 8: Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (ex. when any inputs or outputs exceed the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by $P_{D\max}$ (maximum junction temperature), $\theta_{JA}$ (package junction to ambient thermal resistance), and $T_A$ (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{D\max} = (T_{J\max} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{J\max} = 150^\circ C$, and the typical thermal resistance ($\theta_{JA}$) for board mounting follow:

ADC9708CCN 62°C/W
ADC9708CCJ, ADC9708CMJ 58°C/W

Note 9: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Timing Diagram

![Timing Diagram](image)

FIGURE 1. Equivalent Timing Waveform for Test Circuits and Applications

Note 10: Typicals are at $+25^\circ C$ and represent most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Test Circuits

![Test Circuits](image)

FIGURE 2. Slow Speed Evaluation Circuit for Ratiometric Operation

Note: For evaluation purposes, the ramp start timing generation can be implemented with an LM555 timer (astable operation) or MPU evaluation kit, and a time interval meter for ramp time measurement. The TIM meter will measure the time between 0 to 1 transition of the ramp start and the 1 to 0 transition of the ramp stop. The ramp stop is open collector, and must have an external pull-up resistor to $V_{CC}$.
Test Circuits (Continued)

FIGURE 3. Linearity/Acquisition Time/Conversion Time Test Circuit

FIGURE 4. Static Measurements

Functional Description
This Analog to Digital Converter is a single-slope 8-bit, 6-channel A/D converter that provides all of the necessary analog functions for a microprocessor-based data/control system. The device uses the processor system to provide the necessary addressing, timing and counting functions and includes a 1-of-8 decoder, 8-channel analog multiplexer, sample and hold, precision current reference, ramp integrator and comparator on a single monolithic chip.

Applications that require auto-zero or auto-calibration, (See Figures 5–8) can use selection of address 000 and 111, for input address lines A0–A2, in conjunction with the arithmetic capability of a microprocessor to provide ground and scaling factors. Address 0, 0, 0 internally connects the input of the ramp generator to ground and may be used for zero offset correction in subsequent conversions. Address 1, 1, 1, internally connects the input of the ramp generator to the voltage reference, VREF, and may be used for scale factor correction in subsequent conversions. For the following, refer to the Functional Block Diagram.

Six separate external analog voltage inputs may come into terminals I1–I6 and the specific analog input to be converted is selected via address terminals A0–A2. The analog input voltage level is transferred to the external ramp capacitor connected to pin 4 when the input to the ramp start terminal (pin 3) is at a logic 0 (See Figure 1). The time to charge the capacitor is the acquisition time which is a function of the output impedance of an amplifier internal to the A/D converter and the value of the capacitor. After charging the external capacitor the ramp start terminal is switched to a logic 1 which introduces a high impedance between the analog input voltage and the external capacitor.

The capacitor begins to discharge at a controlled rate. The controlled rate of discharge (ramp) is established by the external reference voltage, the external reference resistor, the value of the external capacitor and the internal leakage of the A/D converter. Connected to the capacitor terminal is a comparator internal to the A/D converter with its output going to the ramp stop terminal (pin 7). The comparator output is a logic one when the capacitor is charged and switches to a logic 0 when the capacitor is in a discharged state. The ramp time is from the time when ramp start goes HIGH (logic ‘1’) to when ramp stop goes LOW (logic ‘0’). The microprocessor must be programmed to determine this conversion time. The ideal (no undesirable internal source impedances, leakage paths, errors on levels where comparator switches or delay time) conversion time is calculated as follows:

$$Ramp\ Time = \frac{V_1 C_H}{I_R}$$

Where $V_1$ = Analog Input Voltage Being Measured
$C_H$ = External Ramp Capacitor
$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$

Where $V_{CC}$ = Power Supply Voltage
$V_{REF}$ = Reference Voltage
$R_{REF}$ = Reference Resistor

In actual use the errors due to a nonideal A/D converter can be minimized by using a microprocessor to make the calculations. (See Figures 5 through 8.)

Channel Selection

<table>
<thead>
<tr>
<th>Input Address Line</th>
<th>Selected Analog Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>A1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
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<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Functional Description (Continued)

Auto-Zero and Full-Scale Features

No Zero Offset TL/H/10409–3
No Full-Scale Error

Count (n) = \frac{V_{IN}}{V_{REF}} \times 256

FIGURE 5. Ideal Transfer Function

\[ N'_{FS} = \frac{V_{IN}}{V_{REF}} \]

\[ N'_{NZ} = N - N'_{FS} \]

\[ N' = (N - N'_{FS}) \times \frac{256}{(N'_{FS} - N'_{NZ})} \]

FIGURE 6. Transfer Function with Zero and Full-Scale Error

FIGURE 7. Transfer Functions with Zero-Correction Added

FIGURE 8. Transfer Function with both Zero and Full-Scale Correction Added

Typical Applications

Application Suggestions and Formulas

1. The capacitor node impedance is approximately 30 \( \mu \Omega \) and should have no parallel resistance for proper operation.
2. \( t_A \) when \( V_{IN} = 0 \) will be finite (i.e., the comparator will always toggle for \( V_{IN} > 0 \)).
3. The ramp stop output is open collector, and an external pull-up resistor is required.
4. All digital inputs and outputs are TTL compatible.
5. For proper operation, timing commences on the 0 to 1 transition of ramp start and terminates on the 1 to 0 transition of ramp stop.
6. \( t_A \geq C_H \times I_A - I_R \times V_{REF} \) (See Figure 1)
7. \( t_R \) (ramp time) = \( C_H \times I_R \times V_{IN} - I_R \times I_{IL_{max}} \times I_R \times V_{REF} \)
(See Figure 1)
8. \( I_R = \frac{V_{CC} - V_{REF}}{R_{REF}} \)

Microprocessor Considerations

Several alternatives exist from a hardware/software standpoint in microprocessor based systems using the ADC9708.

1. The ramp time measurement may be implemented in software using a register increment, followed by a branch back depending on the status of the ramp stop.
2. Alternately, the ramp stop may be tied into the interrupt structure in systems containing a programmable binary timer. This scheme has the following advantages:
   a. The CPU is not committed during the ramp time interval.
   b. It requires only 5 bits of an I/O port for control signals.
Typical Applications (Continued)

3. The auto-zero/auto-full-scale (See Figures 5–8) should use double precision, rounded (as opposed to truncated) arithmetic. Several points are worth noting:
   a. The subtractions are single op code instructions.
   b. The full scale correction uses a multiply by 256 and can be accomplished by a shift left 8 bits (usually one instruction) or placing \((N - N_Z)\) in the MSB register and setting the LSB register to zero, for the double precision divide.
   c. The divisor \((N_{F.S.} - N_Z)\) of the MSB register will always be zero.

These schemes have the following advantages:
   a. No access to the data bus or address bus is required, by the A/D system.
   b. 5 I/O bits completely support the A/D system.
   c. Since auto full scale/auto zero are implemented in software and long term drift (aging) effects are eliminated.
   d. Software overhead is minimal (typically 30 bytes).
   e. Where ratiometric operation is permissible, the 4 external components may be \(\pm 5\%\) tolerance, including the power supply.

Note: \(\Delta V_i = (\text{Applied Force})\) and can be linearized (if necessary) in Software.

FIGURE 9. Ratiometric Strain Gage Sensor/Controller

Applications
Beverage Brewers/Dispensers
Chemical Solution Control
Automatic Liquid Mixing Control

Ramp Current = \(I_R = \frac{V_{CC}}{R_1 + \frac{R_2}{R_3}}\)

\(V_i = \left(\frac{R_{K}}{R_{K} + R_0}\right) V_{CC}\)

Ramp Time = \(T = \frac{V_i}{V_i} \left(\frac{R_2}{R_2 + R_0}\right) \left(1 + \frac{R_2}{R_3}\right) \left(C_{S}R_S\right)\)

FIGURE 10
Physical Dimensions inches (millimeters)

Dual-In-Line Package (J)
Order Number ADC9708CCJ or ADC9708CMJ
NS Package Number J16A
ADC9708 6-Channel 8-Bit μP Compatible A/D Converter

Physical Dimensions inches (millimeters) (Continued)

16 Lead Dual-In-Line Package (N)
Order Number ADC9708CCN
NS Package Number N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.