SDLS167 - OCTOBER 1976 - REVISED MARCH 1988

- 'LS377 and 'LS378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs
- 'LS379 Contains Four Flip-Flops with Double-Rail Outputs
- Individual Data Input to Each Flip-Flop
- Applications Include:

 Buffer/Storage Registers
 Shift Registers

 Pattern Generators

description

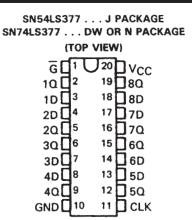
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with an enable input. The 'LS377, 'LS378, and 'LS379 devices are similar to 'LS273, 'LS174, and 'LS175, respectively, but feature a common enable instead of a common clear.

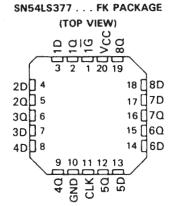
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input \overline{G} is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the \overline{G} input.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 MHz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 10 milliwatts per flip-flop.

FUNCTION TABLE (EACH FLIP-FLOP)

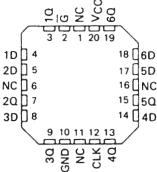
	INPUT	S	оит	PUTS
Ĝ	CLOCK	DATA	Q	ō
Н	X	X	Q ₀	$\bar{\alpha}_0$
L	†	Н	Н	L
L	†	L	L.	н
X	L	X	₫0	$\bar{\alpha}_0$





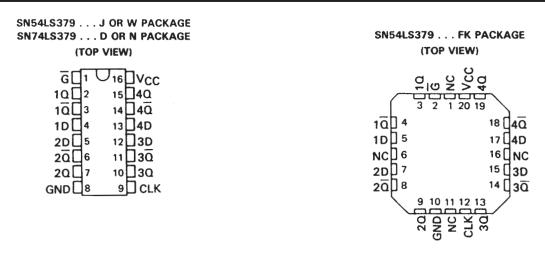
SN54LS378 . . . J OR W PACKAGE SN74LS378 . . . D OR N PACKAGE (TOP VIEW)

SN54LS378 . . . FK PACKAGE (TOP VIEW)



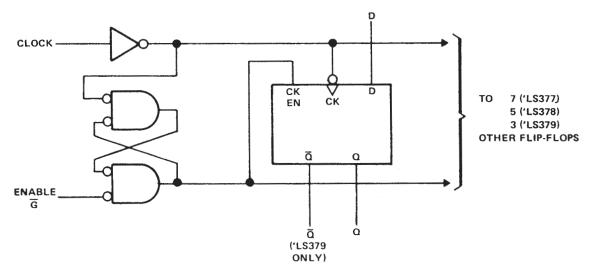
NC - No internal connection



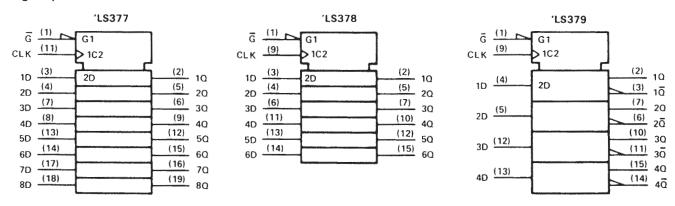


NC - No internal connection

logic diagram (positive logic)



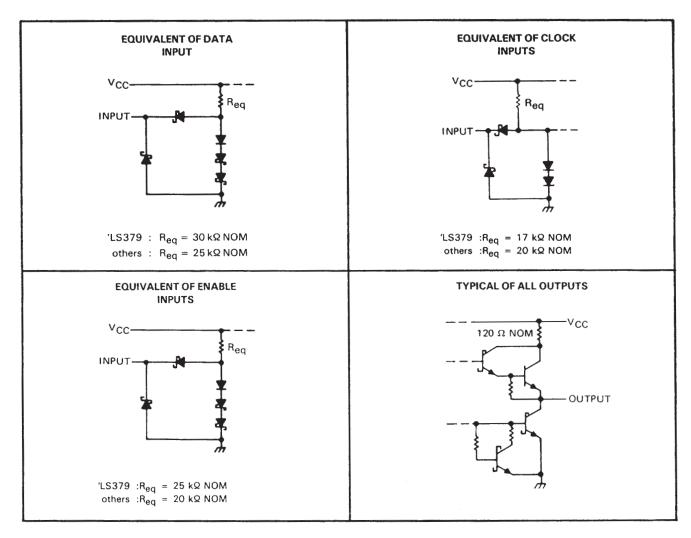
logic symbols†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.



schematics of inputs and outputs



absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)												7 V
Input voltage												7 V
Operating free-air temperature range:	SN54LS'											-55°C to 125°C
	SN74LS'											. 0°C to 70°C
Storage temperature range												-65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5,5	4.75	5	5,25	V
High-level output current, IOH				-400			-400	μΑ
Low-level output current, IOL				4			8	mA
Clock frequency, f _{clock}		0		30	0		30	MHz
Width of clock pulse, t _W		20			20			ns
	Data input	201			201			
Setup time, t _{su}	Enable active-state	251			251			ns
	Enable inactive-state	101			101			1
Hold time, th	Data and enable	51			51	`		ns
Operating free-air temperature, TA		-55		125	0		70	°C

[†]The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TE6	ST CONDITIONS	t		SN54LS	'				
	PANAMETER	163	ST CONDITIONS			TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			2			٧
VIL	Low-level input voltage						0.7			8.0	V
VIK	Input clamp voltage	VCC = MIN,	II = -18 mA				-1.5			-1,5	V
Voн	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{1H} = 2 V, I _{OH} = -400 μA		2.5	3.5		2.7	3.5		٧
VOL	Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max	V _{IH} = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	i V
t _i	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 7 V			1446	0.1			0,1	mA
Ιн	High-level input current	V _{CC} = MAX,	V ₁ = 2.7 V				20			20	μΑ
IIL	Low-level input current	VCC = MAX,	V _I = 0.4 V				-0.4			-0.4	mA
los	Short-circuit output current§	V _{CC} = MAX			-20		-100	-20		-100	mA
			,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	'LS377		17	28		17	28	mΑ
ICC	Supply current	VCC = MAX,	See Note 2	'LS378		13	22		13	22	mΑ
				'LS379		9	15		9	15	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, $TA = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max} Maximum clock frequency	Cլ = 15 pF,	30	40		MHz
tPLH Propagation delay time, low-to-high-level output from clock	R _L = 2 kΩ		17	27	ns
tPHL Propagation delay time, high-to-low-level output from clock	See Note 3		18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{C}$.

[§] Note more than one input should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and ground applied to all data and enable inputs, ICC is measured after a momentary ground, then 4.5 V, is applied to clock.

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interface.ti.com	Digital Control	www.ti.com/digitalcontrol
logic.ti.com	Military	www.ti.com/military
power.ti.com	Optical Networking	www.ti.com/opticalnetwork
microcontroller.ti.com	Security	www.ti.com/security
www.ti.com/lpw	Telephony	www.ti.com/telephony
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interface.ti.com	Digital Control	www.ti.com/digitalcontrol
logic.ti.com	Military	www.ti.com/military
power.ti.com	Optical Networking	www.ti.com/opticalnetwork
microcontroller.ti.com	Security	www.ti.com/security
www.ti.com/lpw	Telephony	www.ti.com/telephony
	Video & Imaging	www.ti.com/video
	Wireless	www.ti.com/wireless
	dataconverter.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com	amplifier.ti.com dataconverter.ti.com dsp.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com www.ti.com/lpw Audio Audio Audio Audio Automotive Broadband Digital Control Military Optical Networking Security Telephony Video & Imaging



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-8992501EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8992501FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-8992501FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/32504B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32504B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32504BRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32504BRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32504BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
JM38510/32504BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN54LS377J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS377J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS378J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS378J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS379J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS379J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS377DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS377N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS377N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS377N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS377NE4	ACTIVE	PDIP	N	20	20	Pb-Free	CU NIPDAU	N / A for Pkg Type
				-	-			3 71 -





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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽
						(RoHS)		
SN74LS377NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS377NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS377NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS377NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS377NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS377NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS377NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS378N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS378N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS378N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS378N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS378NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)		N / A for Pkg Type
SN74LS378NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS378NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN





om 18-Sep-2008

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	n MSL Peak Temp ⁽³⁾
SN74LS378NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS378NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS378NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS378NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS378NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS379D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS379D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS379J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS379J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS379N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS379N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54LS377FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS377FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS377J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS377J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS377W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS377W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS378FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS378FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS378J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS378J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS378W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS378W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS379FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS379FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS379J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS379J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS379W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS379W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

18-Sep-2008

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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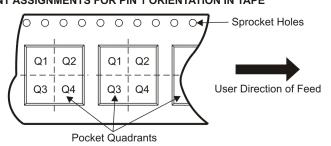
TAPE AND REEL INFORMATION





_		
		Dimension designed to accommodate the component width
ſ	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS377DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS377NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LS378DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS378NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS377DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LS377NSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LS378DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS378NSR	SO	NS	16	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

