SDLS020E - MAY 1990 - REVISED FEBRUARY 2004

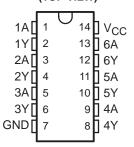
- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

description/ordering information

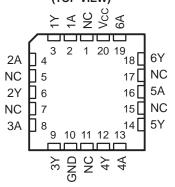
These hex inverter buffers/drivers feature high-voltage open-collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The 'LS06 devices have a rated output voltage of 30 V, and the SN74LS16 has a rated output voltage of 15 V. The maximum sink current for the SN54LS06 is 30 mA, and for the SN74LS06 and SN74LS16 it is 40 mA.

These devices are compatible with most TTL families. Inputs are diode-clamped to minimize transmission effects, which simplifies design. Typical power dissipation is 175 mW, and average propagation delay time is 8 ns.

SN54LS06 . . . J PACKAGE SN74LS06, SN74LS16 . . . D, DB, N, OR NS PACKAGE (TOP VIEW)



SN54LS06 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

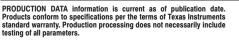
ORDERING INFORMATION

TA	PAC	KAGEŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74LS06N	SN74LS06N
	colo D	Tube	SN74LS06D	1.000
0°C to 70°C	SOIC - D	Tape and reel	SN74LS06DR	LS06
	SOP - NS	Tape and reel	SN74LS06NSR	74LS06
	SSOP - DB	Tape and reel	SN74LS06DBR	LS06
	CDIP – J	Tube	SN54LS06J	SN54LS06J
–55°C to 125°C	CDIF - J	Tube	SNJ54LS06J	SNJ54LS06J
	LCCC - FK	Tube	SNJ54LS06FK	SNJ54LS06FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



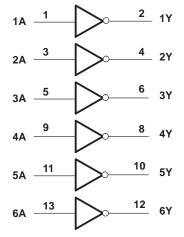
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





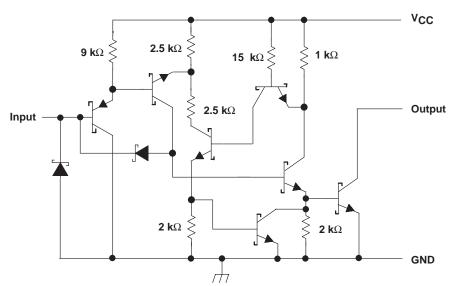
ODESOZOE - MAT 1990 - NE VIOED I EBROART 200

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and NS packages.

schematic (each gate)



Resistor values shown are nominal.

SN54LS06, SN74LS06, SN74LS16 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}		7 V
Input voltage, V _I (see Note 1)		7 V
Output voltage, VO (see Notes 1 and 2): SN54L5	.S06, SN74LS06	30 V
SN74L	.S16	15 V
Package thermal impedance, θ_{JA} (see Note 3):	D package	86°C/W
	DB package	96°C/W
	N package	80°C/W
	NS package	76°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

- 2. This is the maximum voltage that should be applied to any output when it is in the off state.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			s	N54LS06	6		N74LS06 N74LS16		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				8.0			0.8	V
V	LP-de laccal audient callings	'LS06			30			30	.,
VOH	High-level output voltage	SN74LS16						15	V
loL	Low-level output current				30			40	mA
TA	Operating free-air temperature		-55		125	0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	PARAMETER TEST CONDITIONS [‡]			SN54LS06			s s		UNIT	
				MIN	TYP§	MAX	MIN	TYP§	MAX	
VIK	$V_{CC} = MIN,$	$I_{I} = -12 \text{ mA}$				-1.5			-1.5	V
			'LS06, V _{OH} = 30 V			0.25			0.25	A
IOH	$V_{CC} = MIN,$	VIL = 0.8 V	SN74LS16, V _{OH} = 15 V						0.25	mA
			I _{OL} = 16 mA		0.25	0.4		0.25	0.4	
VOL	$V_{CC} = MIN,$	V _{IH} = 2 V	I _{OL} = 30 mA			0.7				V
			$I_{OL} = 40 \text{ mA}$						0.7	
lį	$V_{CC} = MAX$,	V _I = 7 V				1			1	mA
lіН	$V_{CC} = MAX$,	V _I = 2.4 V				20			20	μΑ
I _{IL}	$V_{CC} = MAX$,	V _I = 0.4 V				-0.2			-0.2	mA
ICCH	V _{CC} = MAX					18			18	mA
ICCL	V _{CC} = MAX					60			60	mA

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] All typical values are at V_{CC} = 5 V, and T_A = 25°C.



SN54LS06, SN74LS06, SN74LS16 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS SDLS020E - MAY 1990 - REVISED FEBRUARY 2004

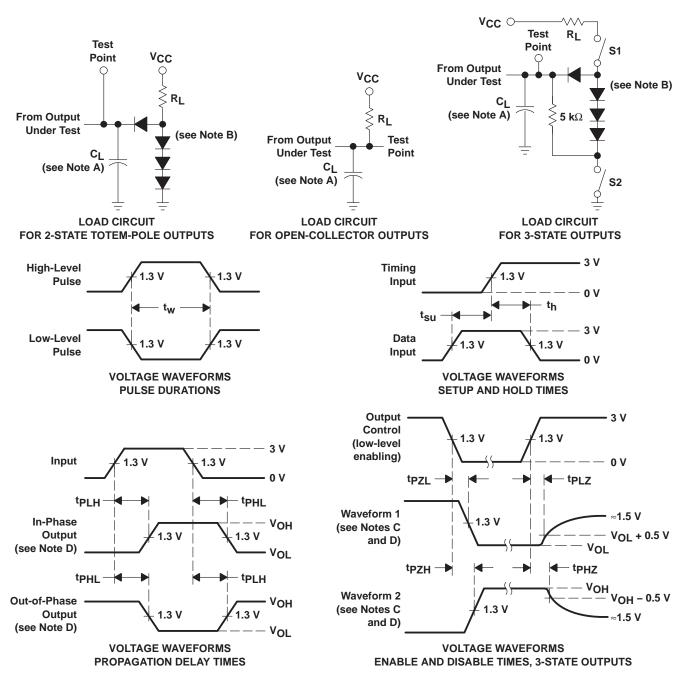
The SN74LS16 is obsolete and is no longer supplied.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
^t PLH	^	V	$R_{I} = 110 \Omega$, $C_{I} = 15 pF$	7	15	20
t _{PHL}	A	Y	$R_L = 110 \Omega$, $C_L = 15 pF$	10	20	ns

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - D. S1 and S2 are closed for tpLH, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.
 - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 - F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O \approx 50~\Omega$, $t_f \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 - G. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms









PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	n MSL Peak Temp ⁽³⁾
5962-9861701Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9861701QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS06J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS06D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LS06DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS06NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS06NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS06NSRG4	ACTIVE	so	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS16D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74LS16DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74LS16N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SNJ54LS06FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS06J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

18-Sep-2008

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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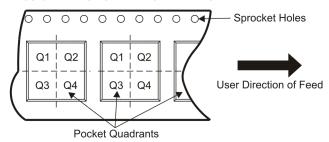
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

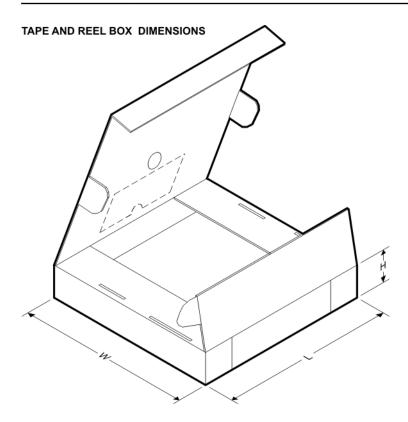
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS06DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LS06DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS06NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS06DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LS06DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS06NSR	SO	NS	14	2000	346.0	346.0	33.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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