- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- ‘122 and ‘LS122 Have Internal Timing Resistors

**description**

These d-c triggered multivibrators feature output pulse-duration control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The ‘122 and ‘LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse duration may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The ‘LS122 and ‘LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

The $R_{int}$ in nominall $10 \, \text{kOhm}$ for ‘122 and ‘LS122.

---

**NOTES:**

1. An external timing capacitor may be connected between $C_{ext}$ and $R_{ext}/C_{ext}$ (positive).
2. To use the internal timing resistor of ‘122 or ‘LS122, connect $R_{int}$ to VCC.
3. For improved pulse duration accuracy and repeatability, connect an external resistor between $R_{ext}/C_{ext}$ and VCC with $R_{int}$ open-circuited.
4. To obtain variable pulse durations, connect an external variable resistance between $R_{int}$ or $R_{ext}/C_{ext}$ and VCC.
NOTE: Retrigger pulses starting before 0.22 C_{ext} (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output duration will remain unchanged.

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

See explanation of function tables on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.
### Logic Diagram (Positive Logic)

#### '122, 'LS122

- **A1** (1)
- **A2** (2)
- **B1** (3)
- **B2** (4)
- **CLR** (5)

![Logic Diagram](image)

- \( R_{int} \)
- \( C_{ext} \)
- \( R_{ext}/C_{ext} \)

\( R_{int} \) is nominally 10 kΩ for '122 and 'LS122.

#### Logic Symbol

![Logic Symbol](image)

- **A1** (1)
- **A2** (2)
- **B1** (3)
- **B2** (4)
- **CLR** (5)
- **RI**
- **CX**

\( Q \)

### Logic Diagram (Positive Logic) (Each Multivibrator)

#### '123, '130, 'LS123

- **A**
- **B**
- **CLR**

![Logic Diagram](image)

- \( R_{ext}/C_{ext} \)
- \( C_{ext} \)

Pin numbers shown are for D, J, N, and W packages.

#### Logic Symbol

![Logic Symbol](image)

- **1A** (1)
- **1B** (2)
- **1CLR** (3)
- **1Cext** (14)
- **1R_{ext}/C_{ext}** (15)
- **2A** (9)
- **2B** (10)
- **2CLR** (11)
- **2Cext** (6)
- **2R_{ext}/C_{ext}** (7)

\( Q \)

\( \bar{Q} \)

\( RX/CX \)

\( CX \)

\( 1Q \)

\( 2Q \)

\( 1Q \)

\( 2Q \)

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
schematics of inputs and outputs

'122, '123, '130 CIRCUITS

**EQUIVALENT OF EACH INPUT**

![Diagram of '122, '123, '130 CIRCUIT](image)

- Clear inputs: $R_{eq} = 2 \, k\Omega$ NOM
- Other inputs: $R_{eq} = 4 \, k\Omega$ NOM

**TYPICAL OF ALL OUTPUTS**

![Diagram of '122, '123, '130 CIRCUIT](image)

- 100 $\Omega$ NOM

'LS122, 'LS123 CIRCUITS

**EQUIVALENT OF EACH INPUT**

![Diagram of 'LS122, 'LS123 CIRCUIT](image)

- 17 $k\Omega$ NOM

**TYPICAL OF ALL OUTPUTS**

![Diagram of 'LS122, 'LS123 CIRCUIT](image)

- 120 $\Omega$ NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

- Supply voltage, $V_{CC}$ (see Note 1) .................................................. 7 V
- Input voltage: '122, '123, '130 .......................................................... 5.5 V
  'LS122, 'LS123 .......................................................... 7 V
- Operating free-air temperature range: SN54' .................................... $-55^\circ C$ to $125^\circ C$
  SN74' ........................................................................... $0^\circ C$ to $70^\circ C$
- Storage temperature range ................................................................ $-65^\circ C$ to $150^\circ C$

**NOTE 1:** Voltage values are with respect to network ground terminal.
### recommended operating conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54' MIN</th>
<th>SN54' NOM</th>
<th>SN54' MAX</th>
<th>SN74' MIN</th>
<th>SN74' NOM</th>
<th>SN74' MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, $V_{CC}$</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>High-level output current, $I_{OH}$</td>
<td>-800</td>
<td></td>
<td></td>
<td>-800</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Low-level output current, $I_{OL}$</td>
<td>16</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Pulse duration, $t_w$</td>
<td>40</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>External timing resistance, $R_{ext}$</td>
<td>5</td>
<td>25</td>
<td>5</td>
<td>5</td>
<td>50</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>External capacitance, $C_{ext}$</td>
<td>No restriction</td>
<td>No restriction</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Wiring capacitance at $R_{ext}/C_{ext}$ terminal</td>
<td>50</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td>µF</td>
</tr>
<tr>
<td>Operating free-air temperature, $T_A$</td>
<td>-55</td>
<td>125</td>
<td>0</td>
<td>70</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

### electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS†</th>
<th>'122 MIN</th>
<th>'122 TYP</th>
<th>'122 MAX</th>
<th>'123 MIN</th>
<th>'123 TYP</th>
<th>'123 MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$ High-level input voltage</td>
<td>$V_{CC} = \min$, $I_I = -12\ mA$</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$ Low-level input voltage</td>
<td></td>
<td>0.5</td>
<td>0.4</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td></td>
<td>0.2</td>
<td>0.4</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_I$ Input current at maximum input voltage</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IH}$ High-level input current</td>
<td></td>
<td>40</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{IL}$ Low-level input current</td>
<td></td>
<td>80</td>
<td>80</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{OS}$ Short-circuit output current§</td>
<td></td>
<td>-10</td>
<td>-10</td>
<td>-10</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$ Supply current (quiescent or triggered)</td>
<td>$V_{CC} = \max$, See Note 5</td>
<td>23</td>
<td>36</td>
<td>46</td>
<td>56</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC} = 5\ V$, $T_A = 25\ ^°C$.
§ Not more than one output should be shorted at a time.

### NOTES:
5. Ground $C_{ext}$ to measure $V_{OH}$ at $Q$, $V_{OL}$ at $\overline{Q}$, or $I_{OS}$ at $\overline{Q}$. $C_{ext}$ is open to measure $V_{OH}$ at $Q$, $V_{OL}$ at $\overline{Q}$, or $I_{OS}$ at $\overline{Q}$.
6. Quiescent $I_{CC}$ is measured (after clearing) with 4.5 V applied to all clear and A inputs, B inputs grounded, all outputs open and $R_{ext} = 25\ \text{k}\Omega$, $R_{int}$ of '122 is open.
7. $I_{CC}$ is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{ext} = 0.02\ \text{µF}$, and $R_{ext} = 25\ \text{k}\Omega$, $R_{int}$ of '122 is open.

### switching characteristics, $V_{CC} = 5\ V$, $T_A = 25\ ^°C$, see note 8

<table>
<thead>
<tr>
<th>PARAMETER††</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>'122, '130 MIN</th>
<th>'122, '130 TYP</th>
<th>'122, '130 MAX</th>
<th>'123 MIN</th>
<th>'123 TYP</th>
<th>'123 MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A</td>
<td>$Q$</td>
<td>$C_{ext} = 0$, $R_{ext} = 5\ \text{k}\Omega$, $C_L = 15\ \text{pF}$, $R_L = 400\ \Omega$</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>33</td>
<td>33</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>A</td>
<td>$Q$</td>
<td>$C_{ext} = 0$, $R_{ext} = 5\ \text{k}\Omega$, $C_L = 15\ \text{pF}$, $R_L = 400\ \Omega$</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>40</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Clear</td>
<td>$Q$</td>
<td>$C_{ext} = 0$, $R_{ext} = 5\ \text{k}\Omega$, $C_L = 15\ \text{pF}$, $R_L = 400\ \Omega$</td>
<td>27</td>
<td>27</td>
<td>27</td>
<td>36</td>
<td>36</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{wQ}$ (min)</td>
<td>A or B</td>
<td>$Q$</td>
<td>$C_{ext} = 1000\ \text{pF}$, $R_{ext} = 10\ \text{k}\Omega$, $C_L = 15\ \text{pF}$, $R_L = 400\ \Omega$</td>
<td>3.08</td>
<td>3.42</td>
<td>3.76</td>
<td>2.76</td>
<td>3.03</td>
<td>3.37</td>
<td>µs</td>
</tr>
</tbody>
</table>

†† $t_{PLH}$ = propagation delay time, low-to-high-level output
§§ $t_{PHL}$ = propagation delay time, high-to-low-level output
$\bullet t_{wQ}$ = duration of pulse at output $Q$.

NOTE 8: Load circuits and voltage waveforms are shown in Section 1.
### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54LS'</th>
<th>SN74LS'</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, $V_{CC}$</td>
<td>MIN</td>
<td>NOM</td>
<td>MAX</td>
</tr>
<tr>
<td></td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td>High-level output current, $I_{OH}$</td>
<td>-400 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-level output current, $I_{OL}$</td>
<td>4 mA</td>
<td></td>
<td>8 mA</td>
</tr>
<tr>
<td>Pulse duration, $t_{PW}$</td>
<td>40 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>External timing resistance, $R_{ext}$</td>
<td>5 kΩ</td>
<td></td>
<td>180 kΩ</td>
</tr>
<tr>
<td>External capacitance, $C_{ext}$</td>
<td>No restriction</td>
<td>No restriction</td>
<td></td>
</tr>
<tr>
<td>Wiring capacitance at $R_{ext}/C_{ext}$ terminal</td>
<td>50 pF</td>
<td></td>
<td>50 pF</td>
</tr>
<tr>
<td>Operating free-air temperature, $T_{A}$</td>
<td>-55°C</td>
<td>125°C</td>
<td>0°C</td>
</tr>
</tbody>
</table>

### Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TEST CONDITIONS†</th>
<th>SN54LS'</th>
<th>SN74LS'</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$ High-level input voltage</td>
<td>$V_{CC} = \text{MIN}$, $I_{I} = -18 , \text{mA}$</td>
<td>2.5 V</td>
<td>3.5 V</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$ Low-level input voltage</td>
<td>$V_{CC} = \text{MIN}$, $V_{IH} = 2 , \text{V}$, $V_{IL} = V_{IH \text{max}}$</td>
<td>0.25 V</td>
<td>0.4 V</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$V_{CC} = \text{MIN}$, $V_{I} = 7 , \text{V}$</td>
<td>0.1 mA</td>
<td>0.1 mA</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{I}$ Input current at maximum input voltage</td>
<td>$V_{CC} = \text{MAX}$, $V_{I} = 7 , \text{V}$</td>
<td>20 mA</td>
<td>20 mA</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OH}$ High-level input current</td>
<td>$V_{CC} = \text{MAX}$, $V_{I} = 2.7 , \text{V}$</td>
<td>20 mA</td>
<td>20 mA</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OL}$ Low-level input current</td>
<td>$V_{CC} = \text{MAX}$, $V_{I} = 0.4 , \text{V}$</td>
<td>-0.4 mA</td>
<td>-0.4 mA</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OS}$ Short-circuit output current‡</td>
<td>$V_{CC} = \text{MAX}$</td>
<td>-20 mA</td>
<td>-100 mA</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$ Supply current (quiescent or triggered)</td>
<td>$V_{CC} = \text{MAX}$, See Note 13</td>
<td>5 LS122</td>
<td>12 LS123</td>
<td>mA</td>
</tr>
</tbody>
</table>

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC} = 5 \, \text{V}$, $T_{A} = 25^\circ\text{C}$.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

### Switching Characteristics, $V_{CC} = 5 \, \text{V}$, $T_{A} = 25^\circ\text{C}$ (See Note 8)

<table>
<thead>
<tr>
<th>Parameter†</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A or B</td>
<td>Q</td>
<td>$C_{ext} = 0$, $C_{L} = 15 , \text{pF}$, $R_{L} = 2 , \text{kΩ}$</td>
<td>23 ns</td>
<td>33 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>A</td>
<td>Q</td>
<td>$C_{ext} = 0$, $C_{L} = 15 , \text{pF}$, $R_{L} = 2 , \text{kΩ}$</td>
<td>23 ns</td>
<td>44 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>B</td>
<td>Q</td>
<td>$C_{ext} = 100 , \text{pF}$, $R_{ext} = 10 , \text{kΩ}$, $R_{L} = 2 , \text{kΩ}$</td>
<td>116 ns</td>
<td>200 ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

†$t_{PLH}$ = propagation delay time, low-to-high-level output
‡$t_{PW}$ = duration of pulse at output Q.

NOTE 8: Load circuits and voltage waveforms are shown in Section 1.
TYPICAL APPLICATION DATA FOR '122, '123, '130

For pulse durations when \( C_{\text{ext}} \leq 1000 \) pF, see Figure 4.

The output pulse duration is primarily a function of the external capacitor and resistor. For \( C_{\text{ext}} > 1000 \) pF, the output pulse duration \( t_w \) is defined as:

\[
t_w = K \cdot R_T \cdot C_{\text{ext}} \left( 1 + \frac{0.7}{R_T} \right)
\]

where

- \( K \) is 0.32 for '122, 0.28 for '123 and '130
- \( R_T \) is in k\( \Omega \) (internal or external timing resistance.)
- \( C_{\text{ext}} \) is in pF
- \( t_w \) is in ns

To prevent reverse voltage across \( C_{\text{ext}} \), it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse duration is:

\[
t_w = K_D \cdot R_T \cdot C_{\text{ext}} \left( 1 + \frac{0.7}{R_T} \right)
\]

where

- \( K_D \) is 0.28 for '122, 0.25 for '123 and '130
- \( R_{\text{ext}} \leq 0.6 \cdot R_{\text{ext, max}} \)

(See recommended operating conditions for \( R_{\text{ext, max}} \).)

Any silicon switching diode such as 1N3064 or equivalent.

Applications requiring more precise pulse durations (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121.

\[\text{TYPICAL OUTPUT PULSE DURATION VS EXTERNAL TIMING CAPACITANCE}\]

\[\text{FIGURE 4}\]

\[\text{†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54 circuits.}\]
TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse duration is essentially determined by the values of external capacitance and timing resistance. For pulse durations when \( C_{\text{ext}} \leq 1000 \) pF, use Figure 6, or use Figure 7 where the pulse duration may be defined as:

\[
t_w = K \cdot R_T \cdot C_{\text{ext}}
\]

When \( C_{\text{ext}} \geq 1 \) \( \mu F \), the output pulse width is defined as:

\[
t_w = 0.33 \cdot R_T \cdot C_{\text{ext}}
\]

For the above two equations, as applicable:

- \( K \) is multiplier factor, see Figure 7
- \( R_T \) is in k\( \Omega \) (internal or external timing resistance)
- \( C_{\text{ext}} \) is in pF
- \( t_w \) is in ns

For maximum noise immunity, system ground should be applied to the \( C_{\text{ext}} \) node, even though the \( C_{\text{ext}} \) node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS122 and 'LS123, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.

'TLS122, 'LS123
TYPICAL OUTPUT PULSE DURATION
VS
EXTERNAL TIMING CAPACITANCE

\[ VCC = 5 \text{ V} \]
\[ TA = 25^\circ \text{C} \]

\[ R_T = 260 \text{ k}\Omega \]
\[ R_T = 160 \text{ k}\Omega \]
\[ R_T = 80 \text{ k}\Omega \]
\[ R_T = 40 \text{ k}\Omega \]
\[ R_T = 20 \text{ k}\Omega \]
\[ R_T = 10 \text{ k}\Omega \]
\[ R_T = 5 \text{ k}\Omega \]

\[ ^t \text{This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.} \]

FIGURE 6
TYPICAL APPLICATION DATA FOR 'LS122, 'LS123†

MULTIPLIER FACTOR vs EXTERNAL CAPACITOR

(K IS INDEPENDENT OF R)

FIGURE 7

DISTRIBUTION OF UNITS vs OUTPUT PULSE DURATION

VCC = 5 V
TA = 25°C

MILDEN
- 20%

+ 20% - ('LS122)

- 8%

+ 8% - ('LS122/
'LS123)

MEDIAN
99% OF UNITS

t_w(out) — Output Pulse Duration

FIGURE 8

VARIATION IN OUTPUT PULSE DURATION vs SUPPLY VOLTAGE

C_ext = 60 pF
R_ext = 10 K ohms
TA = 25°C

FIGURE 9

VARIATION IN OUTPUT PULSE DURATION vs FREE-AIR TEMPERATURE

C_ext = 60 pF
R_T = 10 K ohms

FIGURE 10

NOTE 14: For the 'LS122, the internal timing resistor, R_INT, was used. For the 'LS122/123, an external timing resistor was used for R_T.

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS122 and SN54LS123 only.
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<th>Applications</th>
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# Packaging Information

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<th>Orderable Device</th>
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### PACKAGE OPTION ADDENDUM

18-Sep-2008

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(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **Eco Plan -** The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) **MSL, Peak Temp. --** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

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**REEL DIMENSIONS**

- Reel Diameter

---

**TAPE DIMENSIONS**

- K0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- A0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

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**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

---

*All dimensions are nominal.*

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<td>2500</td>
<td>346.0</td>
<td>346.0</td>
<td>33.0</td>
</tr>
<tr>
<td>SN74LS122NSR</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>346.0</td>
<td>346.0</td>
<td>33.0</td>
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<td>345.9</td>
<td>28.6</td>
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<td>SO</td>
<td>NS</td>
<td>16</td>
<td>2000</td>
<td>346.0</td>
<td>346.0</td>
<td>33.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
### MECHANICAL DATA

**NS (R-PDSO-G**)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

<table>
<thead>
<tr>
<th>Pins</th>
<th>14</th>
<th>16</th>
<th>20</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>10,50</td>
<td>10,50</td>
<td>12,90</td>
<td>15,30</td>
</tr>
<tr>
<td>A MIN</td>
<td>9,90</td>
<td>9,90</td>
<td>12,30</td>
<td>14,70</td>
</tr>
</tbody>
</table>

**NOTES:**

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.
FK (S-CQCC-N**)  
LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

<table>
<thead>
<tr>
<th>NO. OF TERMINALS **</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>20</td>
<td>0.342(8.69)</td>
<td>0.358(9.09)</td>
</tr>
<tr>
<td>28</td>
<td>0.442(11.23)</td>
<td>0.458(11.63)</td>
</tr>
<tr>
<td>44</td>
<td>0.640(16.26)</td>
<td>0.660(16.76)</td>
</tr>
<tr>
<td>52</td>
<td>0.739(18.78)</td>
<td>0.761(19.32)</td>
</tr>
<tr>
<td>68</td>
<td>0.938(23.83)</td>
<td>0.962(24.43)</td>
</tr>
<tr>
<td>84</td>
<td>1.141(28.99)</td>
<td>1.165(29.59)</td>
</tr>
</tbody>
</table>

NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package can be hermetically sealed with a metal lid.  
D. The terminals are gold plated.  
E. Falls within JEDEC MS-004
CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .005 (0.15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0.43) per side.
E. Reference JEDEC MS-012 variation AB.

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 CDFP1–F16 and JEDEC MO–092AC
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\text{Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .005 (0.15) per end.}\]
C. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0.43) per side.
D. Reference JEDEC MS-012 variation AC.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Refer to IPC7351 for alternate board design.  
D. Laser cutting apertures with trapezoidal wall and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
N (R–PDIP–T**)  PLASTIC DUAL–IN–LINE PACKAGE

16 PINs SHOWN

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
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<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
</tbody>
</table>

MS–001 VARIATION

AA
BB
AC
AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\text{Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).}\]
\[\text{The 20 pin end lead shoulder width is a vendor option, either half or full width.}\]

4040049/E 12/2002

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